2.5 V Programmable OmniClock Generator

with Differential LVDS Output

NB3H60113GH3

WDFN8
CASE 511AT

The NB3H60113GH3, which is a member of the OmniClock family, is a one−time programmable (OTP), low power PLL−based clock generator that supports differential 125 MHz frequency output. The device accepts a single ended LVCMOS reference Clock as input. It generates one differential LVDS output. The device can be powered down using the Power Down pin (PD#).

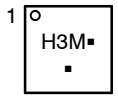
Features

- Member of the OmniClock Family of Programmable Clock Generators
- Operating Power Supply: 2.5 V ± 10%
- I/O Standards
  - Input: LVCMOS Clock
  - Output: LVDS
- 1 Programmable Differential Clock Output of 125 MHz
- Input Frequency Range
  - Reference Clock: 25 MHz
- Power Saving mode through Power Down Pin
- Programming and Evaluation Kit for Field Programming and Quick Evaluation
- Temperature Range −40°C to 85°C
- Packaged in 8−Pin WDFN
- These are Pb−Free Devices

Typical Applications

- Telecom Networks

MARKING DIAGRAM



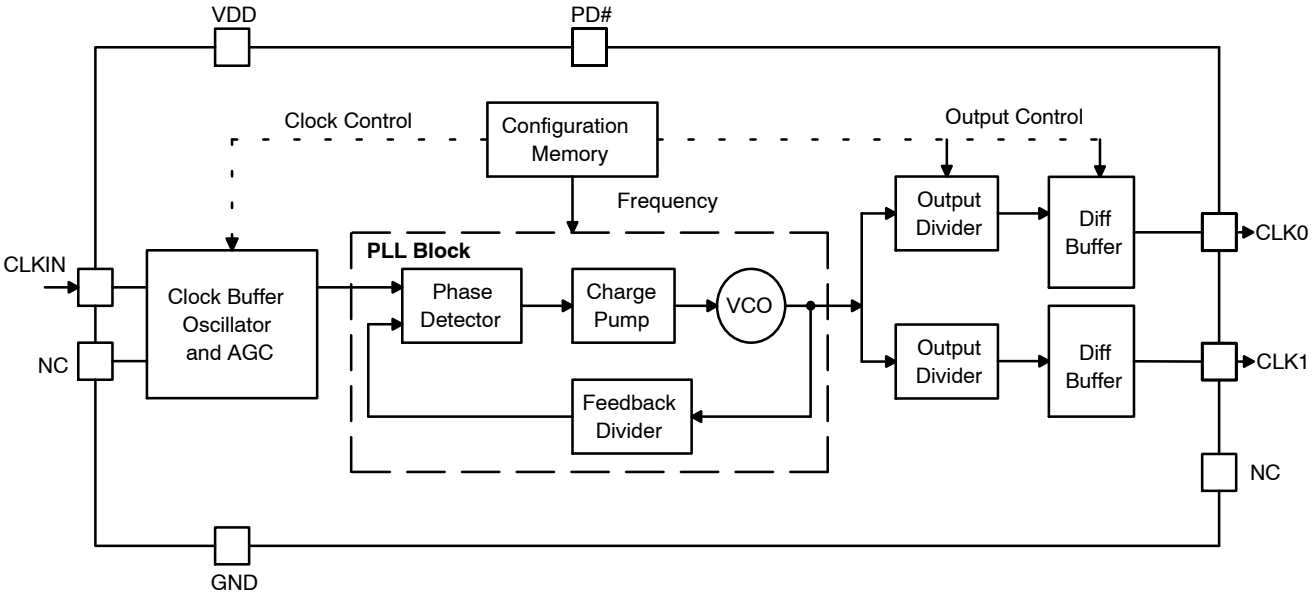
H3 = Specific Device Code
M = Date Code
▪ = Pb−Free Device

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

BLOCK DIAGRAM



Notes:
1. CLK0 and CLK1 can be configured to be LVDS differential output.
2. Dotted lines are the programmable control signals to internal IC blocks.
3. PD# has internal pull down resistor.

Figure 1. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

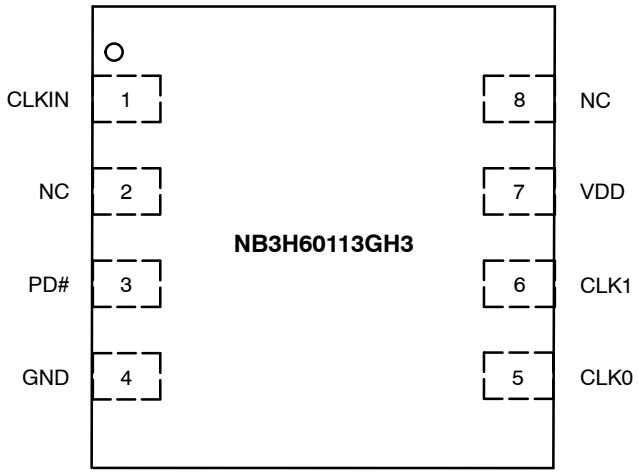


Figure 2. Pin Connections (Top View) – WDFN8

Table 1. PIN DESCRIPTION

Pin No.	Pin Name	Pin Type	Description
1	CLKIN	Input	25 MHz single−ended reference input clock
2	NC	Output	No connect, to be left open floating
3	PD#	Input	Asynchronous LVCMOS input. Active Low Master Reset to disable the device and set outputs Low. Internal pull−down resistor. This pin needs to be pulled High for normal operation of the chip.
4	GND	Ground	Power supply ground
5	CLK0	DIFF Output	Supports 125 MHz LVDS differential signal. The differential outputs will be complementary LOW/HIGH until the PLL has locked and the frequency has stabilized.
6	CLK1	DIFF Output	Supports 125 MHz LVDS differential signal. The differential outputs will be complementary LOW/HIGH until the PLL has locked and the frequency has stabilized.
7	VDD	Power	2.5 V power supply
8	NC	Output	No connect, to be left open floating

Table 2. POWER DOWN FUNCTION TABLE

PD#	Function
0	Device Powered Down
1	Device Powered Up

FUNCTIONAL DESCRIPTION

The NB3H60113GH3 is a 2.5 V programmable differential clock generator, designed to meet the clock requirements for Telecom markets. It has a small package size and it requires low power during operation and while in standby. This device provides the ability to configure a number of parameters as detailed in the following section. The One−Time Programmable memory allows programming and storing of one configuration in the memory space.

Power Supply

Device Supply

The NB3H60113GH3 is designed to work with a 2.5 V VDD power supply. In order to suppress power supply noise it is recommended to connect decoupling capacitors of 0.1 μF and 0.01 μF close to the VDD pin as shown in Figure 3.

Clock Input

Input Frequency

The clock input block can be programmed to use a single ended reference clock source 25 Mhz.

Programmable Clock Outputs

Output Type and Frequency

The NB3H60113GH3 provides one 125 MHz differential output.

Here CLK0 and CLK1 configured for LVDS differential clocking. Refer to the Application Schematic in Figure 3.

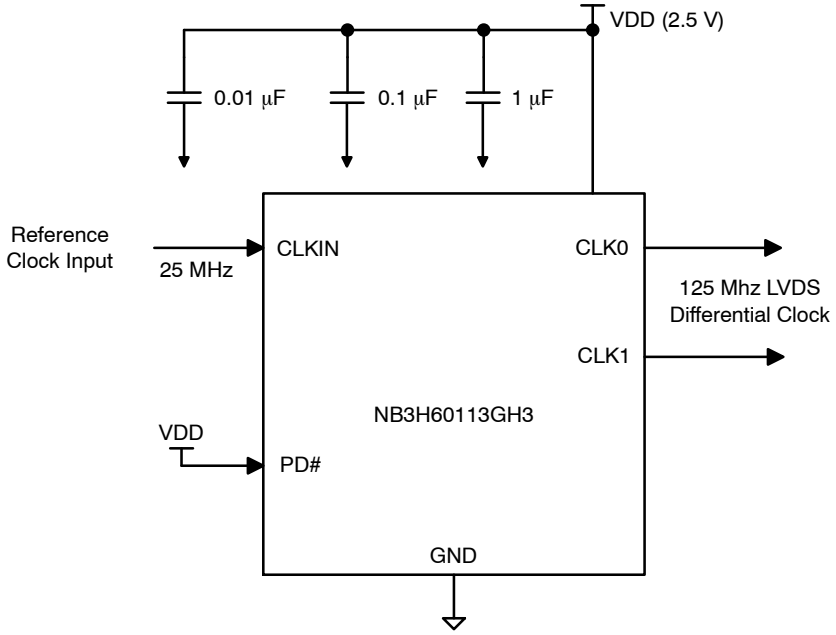


Figure 3. Power Supply Noise Suppression and Differential Output Application setup

Control Inputs

Power Down

Power saving mode can be activated through the power down PD# input pin. This input is an LVCMOS active Low Master Reset that disables the device and sets outputs Low. By default it has an internal pull−down resistor. The chip functions are disabled by default and when PD# pin is pulled high the chip functions are activated.

Configuration Space

NB3H60113GH3 has one Configuration. Table 3 shows the device configuration.

Table 3. EXAMPLE CONFIGURATION

Input Frequency	Output Frequency	VDD	Output Enable	Notes
25 MHz	CLK0 = 125 MHz CLK1 = 125 MHz	2.5 V	CLK0 = Y CLK1 = Y	CLK0/CLK1 = LVDS CLK2: NC

Table 4. ATTRIBUTES

Characteristic	Value
ESD Protection Human Body Model	2 kV
Internal Input Default State Pull up/ down Resistor	50 kΩ
Moisture Sensitivity, Indefinite Time Out of Dry Pack (Note 1)	MSL1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count	130 k
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

Table 5. ABSOLUTE MAXIMUM RATING (Note 2)

Symbol	Parameter		Rating	Unit
VDD	Positive power supply with respect to Ground		−0.5 to +4.6	V
V_I, V_O	Input/Output Voltage with respect to chip ground		−0.5 to VDD + 0.5	V
T_A	Operating Ambient Temperature Range (Industrial Grade)		−40 to +85	°C
T_{STG}	Storage temperature		−65 to +150	°C
T_{SOL}	Max. Soldering Temperature (10 sec)		265	°C
θ_{JA}	Thermal Resistance (Junction−to−ambient) (Note 3)	0 lfpm 500 lfpm	129 84	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−case)		35 to 40	°C/W
T_J	Junction temperature		125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power). ESD51.7 type board. Back side Copper heat spreader area 100 sq mm, 2 oz (0.070 mm) copper thickness.

Table 6. RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Core Power Supply Voltage	2.5 V operation	2.25	2.5	2.75	V
fclkin	Reference Clock Frequency	Single ended clock Input		25		MHz

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 7. DC ELECTRICAL CHARACTERISTICS (V_{DD} = 2.5 V ± 10%; GND = 0 V, T_A = −40°C to 85°C, Notes 4, 9)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$I_{DD\_2.5\ V}$	Power Supply current for core	Configuration Dependent. V_{DD} = 2.5 V, T_A = 25°C, CLKIN = 25 MHz CLK[0:1] = 125 MHz		13		mA
I_{PD}	Power Down Supply Current	PD# is Low to make all outputs OFF			20	μA
V_{IH}	Input HIGH Voltage	Pin XIN	0.65 V_{DD}		V_{DD}	V
		Pin PD#	0.85 V_{DD}		V_{DD}	
V_{IL}	Input LOW Voltage	Pin XIN	0		0.35 V_{DD}	V
		Pin PD#	0		0.15 V_{DD}	
Zo	Nominal Output Impedance	Configuration Dependent		22		Ω
$R_{PUP/PD}$	Internal Pull up/ Pull down resistor	V_{DD} = 2.5 V		80		kΩ

LVDS OUTPUTS (Notes 5 and 6)

V_{OD_LVDS}	Differential Output Voltage		250		450	mV
DeltaV_{OD_LVDS}	Change in Magnitude of VOD for Complementary Output States		0		25	mV
V_{OS_LVDS}	Offset Voltage			1200		mV
Delta V_{OS_LVDS}	Change in Magnitude of VOS for Complementary Output States		0		25	mV
V_{OH_LVDS}	Output HIGH Voltage (Note 7)	V_{DD} = 2.5 V		1425	1600	mV
V_{OL_LVDS}	Output LOW Voltage (Note 8)	V_{DD} = 2.5 V	900	1075		mV
I_{DD_LVDS}		f_{out} = 125 MHz		20		mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Measurement taken with differential clock terminated with test load of 2 pF. See Figure 6.
5. Measured at crossing point where the instantaneous voltage value of the rising edge of CLKx+ equals the falling edge of CLKx−.
6. LVDS outputs require 100 Ω receiver termination resistor between differential pair. See Figure 5.
7. VOHmax = VOSmax + 1/2 VODmax.
8. VOLmax = VOSmin − 1/2 VODmax.
9. Parameter guaranteed by design verification not tested in production.

Table 8. AC ELECTRICAL CHARACTERISTICS (V_{DD} = 2.5 V ± 10%, GND = 0 V, T_A = −40°C to 85°C, Note 10)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fout	Differential Output Frequency			125		MHz
t_{PU}	Stabilization time from Power−up	V_{DD} = 2.5 V with Frequency Modulation		3.0		ms
t_{PD}	Stabilization time from Power Down	Time from falling edge on PD# pin to tri−stated outputs (Asynchronous)		3.0		ms
Eppm	Synthesis Error	Configuration Dependent		0		ppm

DIFFERENTIAL OUTPUT (CLK1, CLK0) (V_{DD} = 2.5 V ±10%; T_A = −40°C to 85°C, Note 10)

$t_{JITTER-2.5\ V}$	Period Jitter Peak−to−Peak	Configuration Dependent. 25 MHz input, f_{out} = 125 MHz, SS off (Notes 10 and 11, see Figure 7)		100		ps
	Cycle−Cycle Peak to Peak Jitter	Configuration Dependent. 25 MHz input, f_{out} = 125 MHz, SS off (Notes 10, and 11, see Figure 7)		100		ps
$t_{r\ 2.5\ V}$	Rise Time	Measured between 20% to 80% V_{DD} = 2.5 V LVDS	175		700	ps
$t_{f\ 2.5\ V}$	Fall Time	Measured between 20% to 80% V_{DD} = 2.5 V LVDS	175		700	ps
t_{DC}	Output Clock Duty Cycle	V_{DD} = 2.5 V; Duty Cycle of Ref clock is 50%				%
		PLL Clock	45	50	55	
		Reference Clock	40	50	60	

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

10. AC performance parameters like jitter change based on the output frequency, spread selection, power supply and loading conditions of the output. For application specific AC performance parameters, please contact **onsemi**.
11. Period jitter Sampled with 10000 cycles, Cycle−cycle jitter sampled with 1000 cycles. Jitter measurement may vary. Actual jitter is dependent on Input jitter and edge rate, number of active outputs, inputs and output frequencies, supply voltage, temperature, and output load.

SCHEMATIC FOR OUTPUT TERMINATION

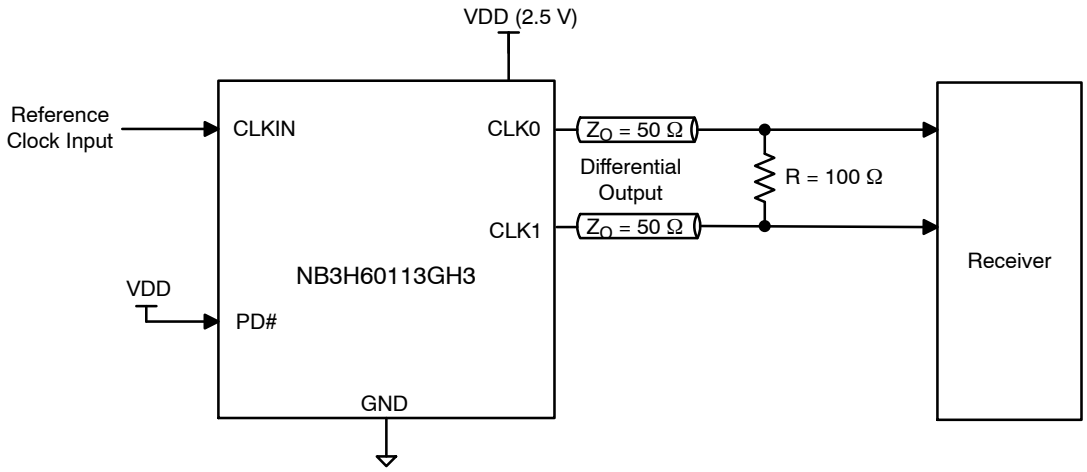


Figure 4. Typical Termination for Differential Signaling Device Load

PARAMETER MEASUREMENT TEST CIRCUITS

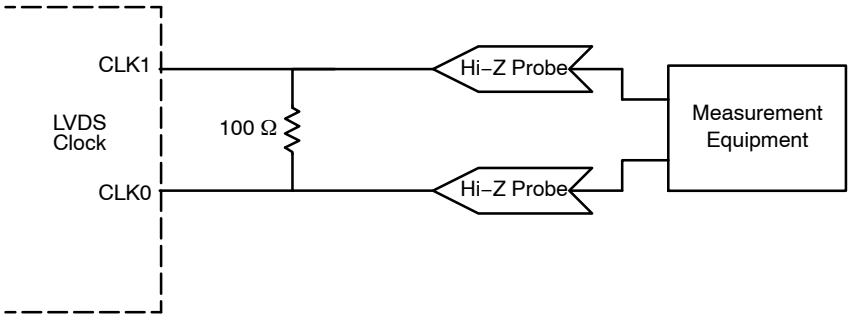


Figure 5. LVDS Parameter Measurement

TIMING MEASUREMENT DEFINITIONS

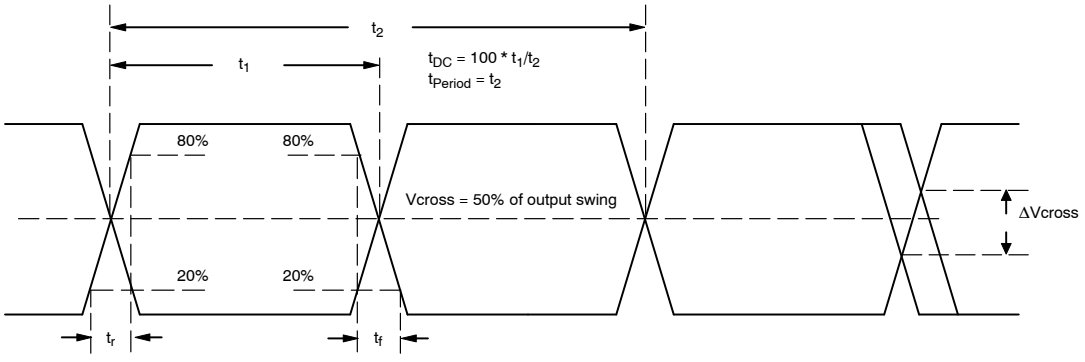


Figure 6. Differential Measurement for AC Parameters

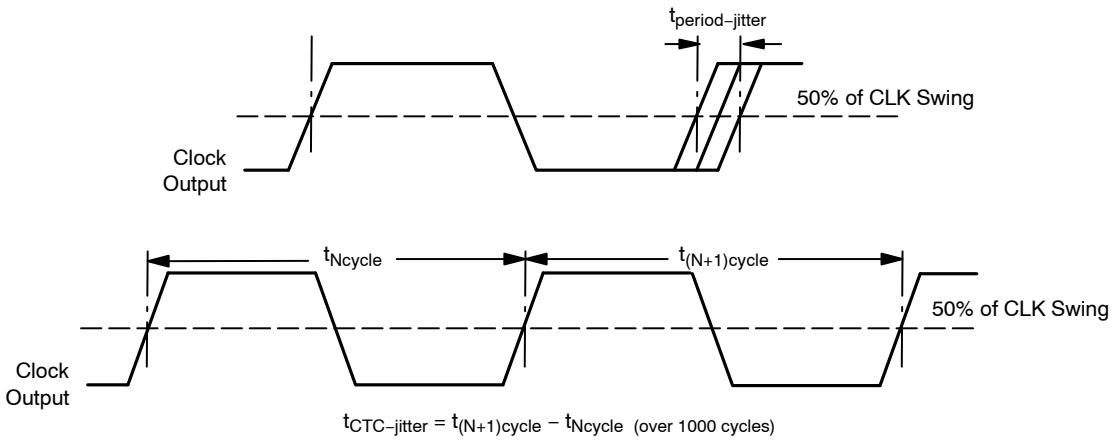


Figure 7. Period and Cycle−Cycle Jitter Measurement

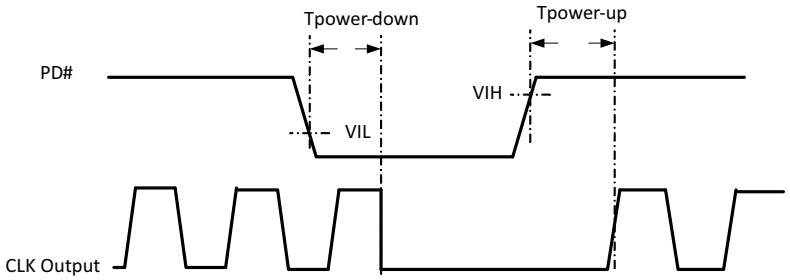


Figure 8. Output Enable/ Disable and Power Down Functions

APPLICATION GUIDELINES

Output Interface and Terminations

The NB3H60113GH3 consists of a Output Driver to support LVDS standards. Termination techniques required is as shown in Figure 4.

LVDS Interface

Differential signaling like LVDS has inherent advantage of common mode noise rejection and low noise emission, and thus a popular choice clock distribution in systems. TIA/EIA−644 or LVDS is a standard differential, point−to−point bus topology that supports fast switching speeds and has benefit of low power consumption. The driver consists of a low swing differential with constant current of 3.5 mA through the differential pair, and generates switching output voltage across a 100 Ω terminating resistor (externally connected or internal to the receiver). Power dissipation in LVDS standard ($(3.5\ mA)^2$ x 100 Ω = 1.2 mW) is thus much lower than other differential signalling standards.

A fan−out LVDS buffer (like **onsemi**'s NB6N1xS and NB6L1xS) can be used as an extension to provide clock signal to multiple LVDS receivers to drive multiple point−to−point links to receiving node.

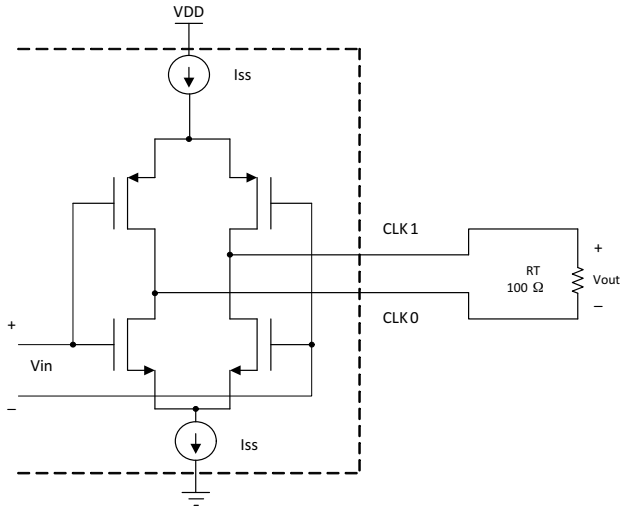


Figure 9. Simplified LVDS Output Structure with Termination

Recommendation for Clock Performance

Clock performance is specified in terms of Jitter in time the domain and Phase noise in frequency domain. Details

and measurement techniques of Cycle−cycle jitter, period jitter, TIE jitter and Phase Noise are explained in application note AND8459/D.

In order to have a good clock signal integrity for minimum data errors, it is necessary to reduce the signal reflections. Reflection coefficient can be zero only when the source impedance equals the load impedance. Reflections are based on signal transition time (slew rate) and due to impedance mismatch. Impedance matching with proper termination is required to reduce the signal reflections. The amplitude of overshoots is due to the difference in impedance and can be minimized by adding a series resistor (Rs) near the output pin. Greater the difference in impedance, greater is the amplitude of the overshoots and subsequent ripples. The ripple frequency is dependant on the signal travel time from the receiver to the source. Shorter traces results in higher ripple frequency, as the trace gets longer the travel time increases, reducing the ripple frequency. The ripple frequency is independent of signal frequency, and only depends on the trace length and the propagation delay. For eg. On an FR4 PCB with approximately 150 ps/ inch of propagation rate, on a 2 inch trace, the ripple frequency = 1 / (150 ps * 2 inch * 5) = 666.6 MHz; [5 = number of times the signal travels, 1 trip to receiver plus 2 additional round trips]

PCB traces should be terminated when trace length tr/f / (2* tprate); tr/f = rise/ fall time of signal, tprate = propagation rate of trace.

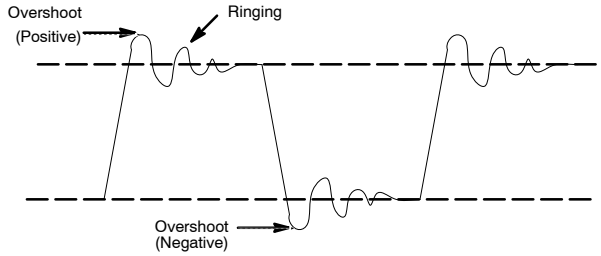


Figure 10. Signal Reflection Components

PCB Design Recommendation

For a clean clock signal waveform it is necessary to have a clean power supply for the device. The device must be isolated from system power supply noise. A 0.1 μF and a 2.2 μF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to VDD pin and the ground via should be kept thicker and as short as possible. All the VDD pins should have decoupling capacitors.

Stacked power and ground planes on the PCB should be large. Signal traces should be on the top layer with minimum vias and discontinuities and should not cross the reference planes. The termination components must be placed near the source or the receiver. In an optimum layout all components are on the same side of the board, minimizing vias through other signal layers.

Device Applications

The NB3H60113GH3 is targeted mainly for the Telecom market segment and can be used as per the examples below Figure 11.

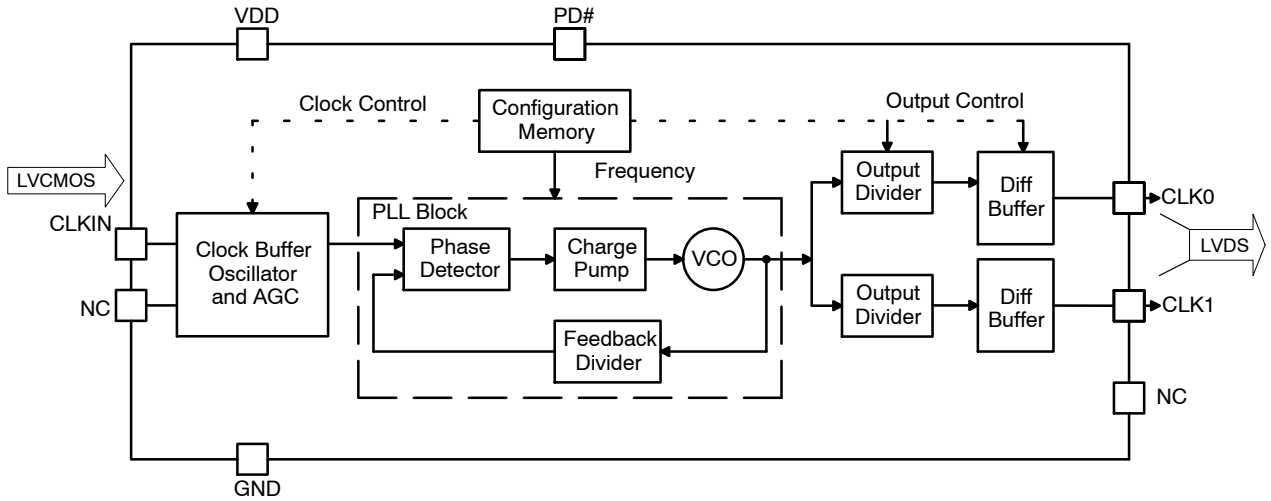


Figure 11. Application as Level Translator

NOTE: LVCMOS signal level cannot be translated to a higher level of LVCMOS voltage.

ORDERING INFORMATION

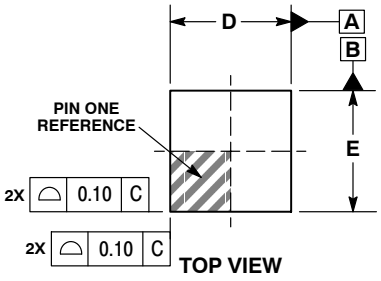
Device	Case	Package	Shipping†
NB3H60113GH3MTR2G	511AT	DFN−8 (Pb−Free)	3000 / Tape & Reel

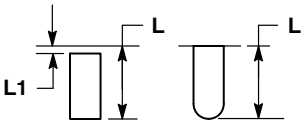
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NB3H60113GH3

PACKAGE DIMENSIONS

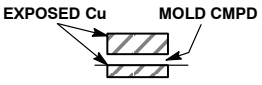
WDFN8 2x2, 0.5P
CASE 511AT−01
ISSUE O



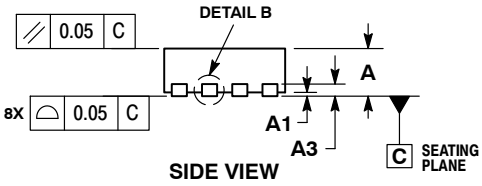


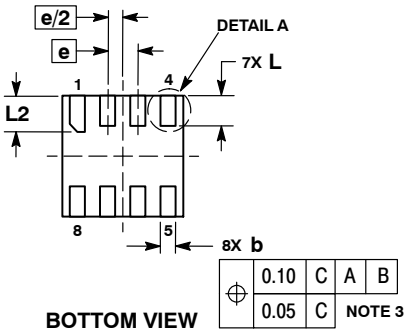
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
E	2.00 BSC	
e	0.50 BSC	
L	0.40	0.60
L1	---	0.15
L2	0.50	0.70

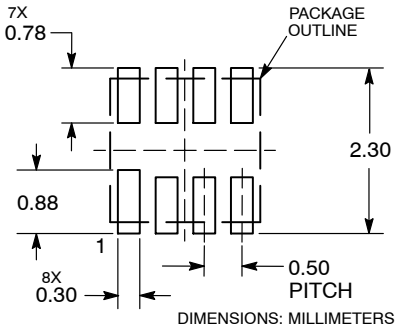


DETAIL B
ALTERNATE CONSTRUCTIONS





RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

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