MOSFET Basic

AN-9010/D

SUMMARY

The Bipolar Power Transistor (BPT), as a switching device for power applications, had a few disadvantages. This led to the development of the power Metal Oxide Semiconductor Field Effect Transistor (MOSFET). The power MOSFET is used in applications such as Switched Mode Power Supplies (SMPS), computer peripherals, automotive, and motor control. Continuous research has improved its characteristics for replacing the BJT. This application note is a general description of power MOSFETs and a presentation of some of **onsemi**'s product specifications.

HISTORY

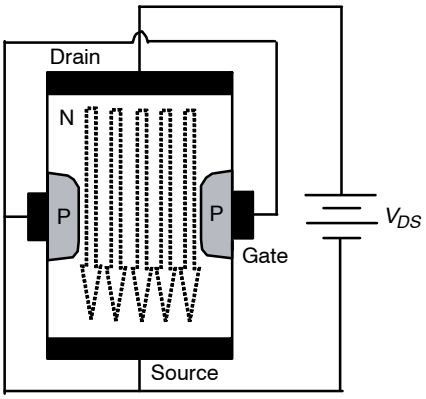
The theory behind the Field Effect Transistor (FET) has been known since 1920~1930, which is 20 years before the bipolar junction transistor was invented. At that time, J.E. Lilienfeld of the USA suggested a transistor model having two metal contacts on each side with a metallic plate (aluminum) on top of the semiconductor. The electric field at the semiconductor surface, formed by the voltage supplied at the metallic plate, enables the control of the current flow between the metal contacts. This was the initial concept of the FET. Due to lack of appropriate semiconductor materials and immature technology, development was very slow. William Shockely introduced Junction Field Effect Transistors (JFETs) in 1952. Dacey and Ross improved on it in 1953. In JFETs, Lilienfeld's metallic field is replaced by a P−N junction, the metal contacts are called source and drain, and the field effect electrode is called a gate. Research in small−signal MOSFETs continued without any significant improvements in power MOSFET design, until new products were introduced in the 1970s.

In March of 1986, Fairchild® formed with nine people and began research on power MOSFETs. 1990's, Fairchild has developed a QFET® devices using planar technology and low−voltage POWERTRENCH® products using trench technology.

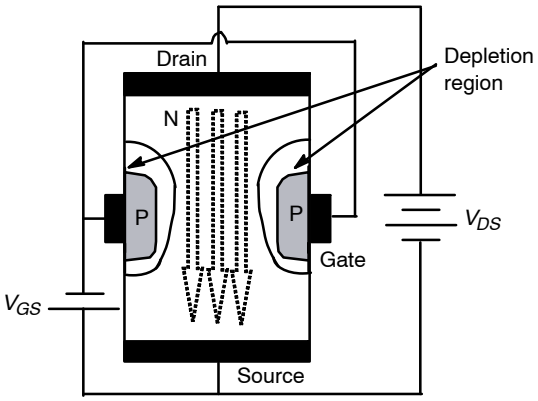
FETS

Junction Field Effect Transistors (JFETs)

There are two types of JFETs: an N−channel type and a P−channel type. They both control the drain−to−source current by the voltage supplied to the gate. As shown in Figure 1 (a) , if the bias is not supplied at the gate, the current flows from the drain to the source. When the bias is supplied at the gate, the depletion region begins to grow and reduces the current, as shown in Figure 1 (b). The reason for the wider depletion region of the drain, compared to the source depletion region, is that the reverse bias of the gate and the drain, V_{DG} (= V_{GS} + V_{DS}), is higher than the bias between the gate and the source, V_{GS}.



(a) VGS (Gate−Source Voltage) is Not Supplied

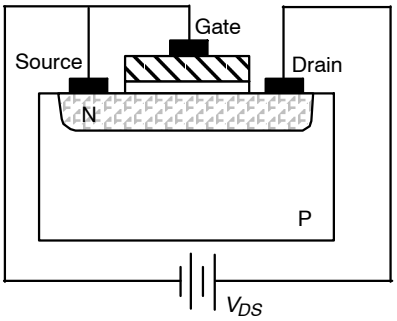


(b) VGS (Gate−Source Voltage) is Supplied

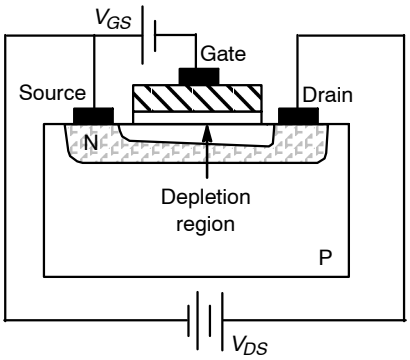
Figure 1. Structure of JFET and Its Operation

Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)

The two types of MOSFETs are depletion type and enhancement type, and each has a N/P−channel type. The depletion type is normally on and operates as a JFET *(refer to Figure 2)*. The enhancement type is normally off, which means that the drain−to−source current increases as the voltage at the gate increases. No current flows when no voltage is supplied at the gate *(refer to Figure 3)*.

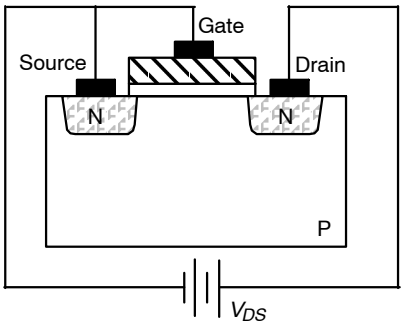


(a) VGS Gate−Source Voltage is Not Supplied

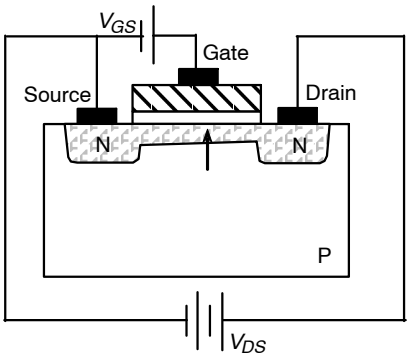


(b) VGS (Gate−Source Voltage) is Supplied

Figure 2. Structure of a Depletion Type MOSFET and Its Operation



(a) VGS (Gate−Source Voltage) is Not Supplied



(b) VGS (Gate−Source Voltage) is Supplied

Figure 3. Structure of a Enhancement Type MOSFET and Its Operation

STRUCTURE OF A MOSFET

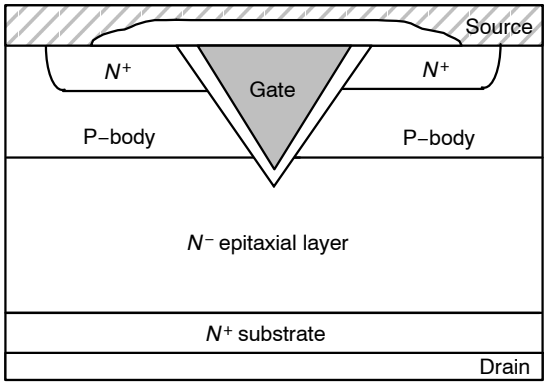
Lateral Channel Design

The drain, gate, and source terminals are placed on the surface of a silicon wafer. This is suitable for integration, but not for obtaining high power ratings because the distance between source and drain must be large to obtain better voltage blocking capability. The drain−to−source current is inversely proportional to the length.

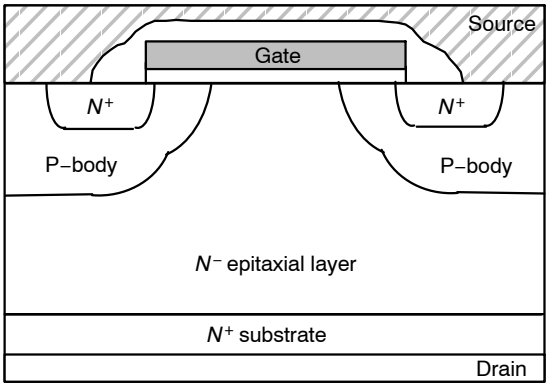
Vertical Channel Design

The drain and source are placed on the opposite sides of a wafer. This is suitable for a power device, as more space can be used as source. As the length between the source and drain is reduced, it is possible to increase the drain−to−source current rating and increase the voltage blocking capability by growing the epitaxial layer (drain drift region).

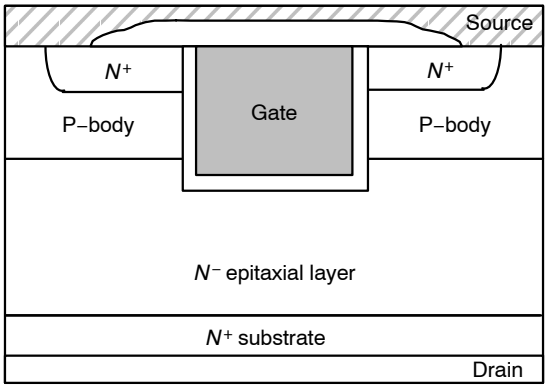
1. The VMOSFET Design: the first to be commercialized, this design was has a V−groove at the gate region, as shown in Figure 4 (a). Due to stability problems in manufacturing and a high electric field at the tip of the V−groove, VMOSFETs were replaced by DMOSFETs.
2. The DMOSFET Design: has a double−diffusion structure with a P−base region and a N^+ source region, as shown in Figure 4 (b). It is the most commercially successful design.
3. The UMOSFET Design: As shown in Figure 4 (c), this design has a U−groove at the gate region. Higher channel density reduces the on−resistance as compared to the VMOSFETs and the DMOSFETs. UMOSFET designs with the trench etching process were commercialized in the 90's.



(a) VMOSFET Vertical



(b) DMOSFET Vertical



(c) UMOSFET Vertical

Figure 4. Vertical Channel Structure

CHARACTERISTICS OF A MOSFET

Advantages

High Input Impedance − Voltage−Controlled Device − Easy to Drive

To maintain the on−state, a base drive current 1/5th or 1/10th of collector current is required for the current−controlled device (BJT). A larger reverse base drive current is needed for the high−speed turn−off of the current−controlled BJT. Due to these characteristics, base drive circuit design becomes complicated and expensive. On the other hand, a voltage−controlled MOSFET is a switching device driven by a channel at the semiconductor's surface due to the field effect produced by the voltage applied to the gate electrode, which is isolated from the semiconductor surface. Because the required gate current during switching transient, as well as the on and off states, is small; the drive circuit design is simpler and less expensive.

UniPolar Device − Majority Carrier Device − Fast Switching Speed

Wide Safe Operating Area (SOA)

It has a wider SOA than the BJT because high voltage and current can be applied simultaneously for a short duration. This eliminates destructive device failure due to second breakdown.

Forward−Voltage Drop with Positive Temperature Coefficient − easy to use in Parallel

When the temperature increases, forward−voltage drop also increases. This causes the current to flow equally through each device when they are in parallel. Hence, the MOSFET is easier to use in parallel than the BJT, which has a forward− voltage drop with a negative temperature coefficient.

Disadvantage

In high breakdown voltage devices over 200 V, the conduction loss of a MOSFET is larger than that of a BJT, which has the same voltage and current rating due to the on−state voltage drop.

Basic Characteristics

- Vertically oriented four−layer structure ($N^+ P N^- N^+$)
- Parasitic BJT exists between the source and the drain.

The P−type body region becomes base, the N^+ source region becomes an emitter and the N−type drain region becomes the collector *(refer to Figure 5)*. The breakdown voltage decreases from BV_{CBO} to BV_{CEO}, which is 50 ~ 60% of BV_{CBO} when the parasitic BJT is turned on. In this state, if a drain voltage higher than BV_{CEO} is supplied, the device falls into an avalanche breakdown state. If the drain current is not limited externally, it is destroyed by the second breakdown. The N^+ source region and the P−type body region must be shorted by metallization to prevent the parasitic BJT from turning on.

If the V_{DS} rate of increase is large in the high speed turn−off state, there is a voltage drop between the base and the emitter, which causes the BJT to turn on. This is prevented by increasing the doping density of the P− body region, which is at the bottom of the N^+ source region, and by lowering the MOSFETs switching speed, by designing the circuit so that the gate resistance is large. Due to the source region being short, another parasitic component, the diode, is formed. This is used in half− and full−bridge converters.

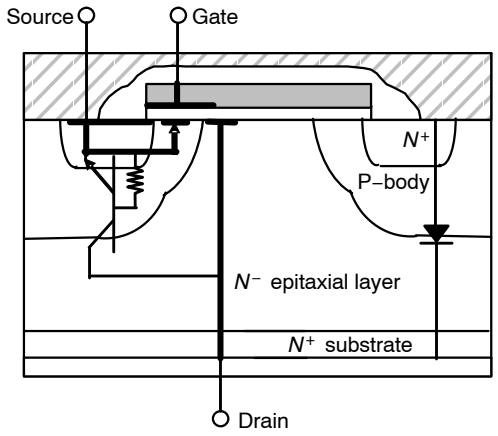


Figure 5. MOSFET Vertical Structure Showing Parasitic BJT and Diode

Output Characteristics

I_D characteristics are due to V_{DS} in many V_{GS} conditions *(refer to Figure 6)*.

→ It is divided into the ohmic region, the saturation (= active) region, and the cut−off region.

Table 1. OUTPUT CHARACTERISTICS REGIONS

Ohmic Region	A constant resistance region. If the drain−to−source voltage is zero, the drain current also becomes zero regardless of gate−to−source voltage. This region is at the left side of the $V_{GS} - V_{GS(th)} = V_{DS}$ boundary line ($V_{GS} - V_{GS(th)} > V_{DS} > 0$). Even if the drain current is very large, in this region the power dissipation is maintained by minimizing $V_{DS(on)}$.
Saturation Region	A constant−current region. It is at the right side of the $V_{GS} - V_{GS(th)} = V_{DS}$ boundary line. Here, the drain current differs by the gate−to−source voltage, and not by the drain−to−source voltage. Hence, the drain current is called saturated.
Column Head	Called the cut−off region because the gate−to−source voltage is lower than the $V_{GS(th)}$ (threshold voltage).

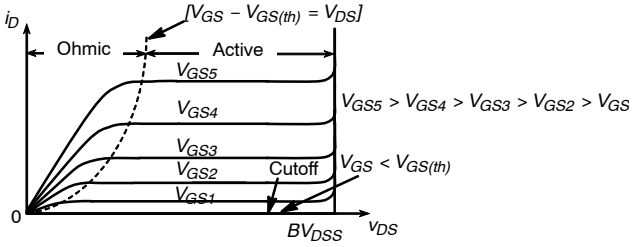


Figure 6. Output Characteristics

Transfer Characteristics

i_D characteristics due to V_{GS} in the active region (*refer to Figure 7*).

I_D equation due to V_{GS}:

$$i_D = K\left(v_{GS} - V_{GS(th)}\right)^2$$

$$K = \mu_n C_{OX} \frac{W}{2L} \qquad \text{(eq. 1)}$$

where

μn is majority−carrier mobility;

C_{OX} is gate oxide capacitance per unit area;

$C_{OX} = \varepsilon_{OX} / t_{OX}$;

ε_{OX} is dielectric constant of the silicon dioxide;

t_{OX} is thickness of the gate oxide;

W is channel width; and

L is channel length.

A parabolic transfer curve exists in a logic−level device according to Equation 1. In a power MOSFET, this is true only in the low ID of the transfer curve and the other areas show linearity. This is because the mobility of the carrier is not constant, but decreases due to the increase of the electric field along with the increase of ID at the inverse layer.

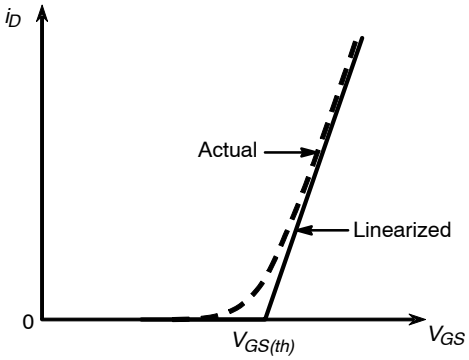


Figure 7. Transfer Curve

CHARACTERISTICS OF MOSFET IN ON AND OFF STATE

OFF State

BV_{DSS}

This is the maximum drain−to−source voltage the MOSFET can endure without the avalanche breakdown of the body− drain P−N junction in off state (where the gate and source are shorted). The measurement conditions are V_{GS} = 0 V, I_D = 250 μA, and the drift region's (N− epitaxy) length is determined by the BVDSS. Avalanche, reach−through, punch−through, Zener, and dielectric breakdowns are the factors that drive breakdown. Three of these factors are described below:

Avalanche Breakdown:

The mobile carriers' sudden avalanche breakdown caused by the increasing electric field in the depletion region of the body−drain P−N junction up to a critical value. It is the main factor among others that drives breakdown.

Reach−Through Breakdown:

A special case of avalanche breakdown occurring when the depletion region of the N− epitaxy contacts the N^+ substrate.

Punch−Through Breakdown:

An avalanche breakdown occurring when the depletion region of the body−drain junction contacts the N^+ source region.

I_{DSS}

The drain−to−source leakage current when it is an off state where the gate is being shorted with the source. The increase in I_{DSS}, which is sensitive to temperature, is large with the increase in temperature, while the increase in BV_{DSS} is very little.

Turn−On Transient

Process of Channel Formation

When a small positive gate−to−source voltage is supplied to the gate electrode *(refer to Figure 8 (a))*.

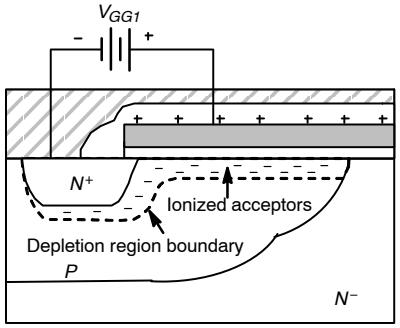
A positive charge induced in the gate electrode inducts the same amount of negative charge at the oxide – silicon interface (P−−body region, which is underneath the gate oxide). The holes are pushed into the semiconductor bulk by an electric field and the depletion region is formed by the acceptors with a negative charge.

Formation of the Inversion Layer:

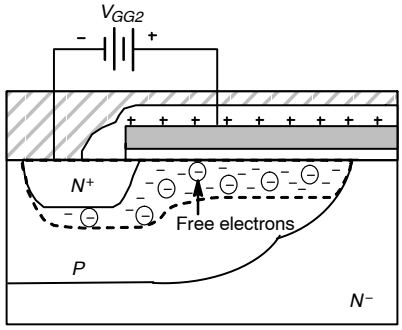
As the positive gate−to−source voltage increases *(refer to Figure 8 (b) and Figure 8 (c))*, the depletion region becomes wider towards the body and begins to drag the free electrons to the interface. These free electrons are created by thermal ionization. The free holes, created with free electrons, are pushed into the semiconductor bulk. The holes that have not been pushed into the bulk are neutralized by the electrons that have been dragged by the positive charge of the holes from the N^+ source. If the supplied voltage keeps increasing, the density of the free holes of the body and the free electrons of the interface becomes equal. At this point, the free electron layer is called an inversion layer. The inversion layer enables the current flow by becoming the conductive pass (= channel) of the MOSFETs drain and source.

Threshold Voltage:

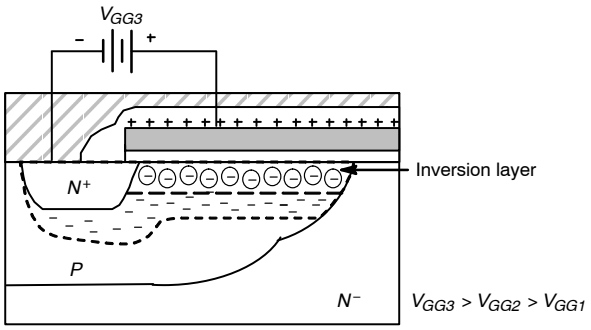
The gate−to−source voltage, which forms the inverse layer, is called VGS(th) (= threshold voltage).



(a) Formation of Depletion Region



(b) Formation of Inversion Layer

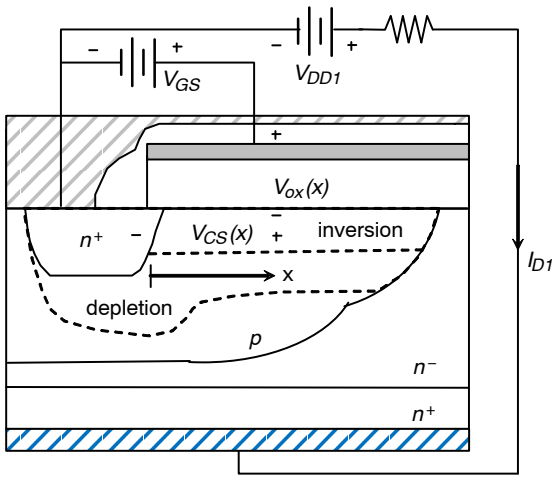


(c) Formation of Inversion Layer

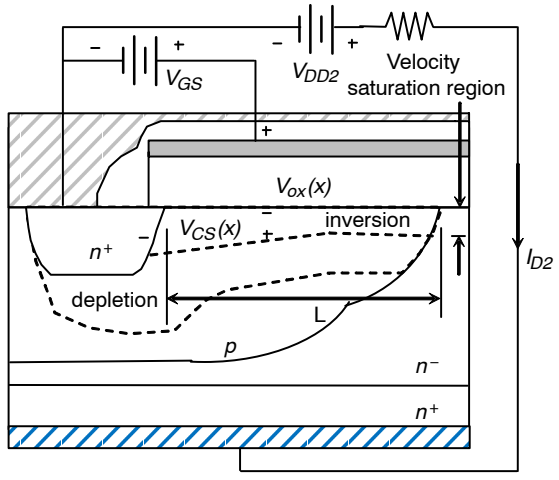
Figure 8. Process of Channel Formation

ON State

Drain current (I_D) changes due to the increase in drain−to−source voltage (V_{DD}) (V_{GS} is constant). I_D starts to flow when the channel has formed and V_{DD} is supplied. When the V_{GS} is a constant value and the V_{DD} is increased, the I_D also increases linearly. As shown in the MOSFET output characteristics graph, when the real V_{DD} goes over a certain level, the rate of increase in I_D decreases slowly. Eventually, it becomes a constant value independent of V_{DD} and becomes dependent on V_{GS}.



(a) Spatially Uniform



(b) Spatially Non−Uniform

Figure 9. Inversion Layer Thickness Changes due to the Increase of the Drain−to−Source Voltage (V_{DD}) where $V_{DD1} < V_{GS} - V_{GS(th)}$, $V_{DD2} > V_{GS} - V_{GS(th)}$, I_{D2} (Saturation Current) > I_{D1}

To understand the characteristics, shown in Figure 9, note the voltage drop at $V_{CS}(x)$ due to ohmic resistance when ID is flowing at the inverse layer. $V_{CS}(x)$ is the channel−to−source voltage from the source at a distance of x. This voltage is equal to the V_{GS}–$V_{ox}(x)$ at all x points. $V_{ox}(x)$ is the gate−to−body voltage crossing the gate oxide from the source at a distance of x and it has the maximum value at V_{DS} at x = L (the drain end of the channel). As shown in Figure 9 (a), when low voltage $V_{DD} = V_{DD1}$ is supplied, low I_D (= I_{D1}), which has almost no voltage drop of $V_{CS}(x)$, flows. As $V_{ox}(0) \sim V_{ox}(L)$ is constant, the thickness of the inversion layer remains uniform. As higher V_{DD} is supplied, I_D increases, the voltage drop of $V_{CS}(x)$ occurs, and the value of $V_{ox}(x)$ decreases. These reduce the thickness of the inversion layer starting from x = L. Because of this, the resistance increases and the graph of I_D starts to become flat, as opposed to increasing with the increment of V_{DD}. When $V_{ox}(L) = V_{GS} - V_{DS} = V_{GS(th)}$, as I_D increases, the inversion layer at x = L doesn't disappear due to the high electric field ($J = \sigma E$) formed by the reduction in thickness, and maintains the minimum thickness. The high electric field not only maintains the minimum thickness of the inversion layer, it also saturates the velocity of the charge carrier at $V_{ox}(L) = V_{GS} - V_{DS} = V_{GS(th)}$.

The velocity of the charge carrier increases with the increase in the electric field initially and, at a certain point, is saturated. Silicon starts saturating when the electric field reaches 1.5 x 10^4 [V/cm] and the drift velocity of the electron is 8 x 106 [cm/s]. At this point, the device goes into the active region. When a higher V_{DD} is supplied, as shown in Figure 9 (b), the electric field at x = L increases more and the channel region that maintained the minimum thickness expands towards the source. V_{DS} becomes $V_{DS} > V_{GS} - V_{GS(th)}$, due to the increase of V_{DD}, and I_D is kept constant.

Turn−off Transient

The reverse process of the turn−on transient described above is the turn−off transient.

User's manual

Characteristics of Capacitance

The three types of parasitic capacitance are:

- Input capacitance: $C_{iss} = C_{gd} + C_{gs}$
- Output capacitance: $C_{oss} = C_{gd} + C_{ds}$
- Reverse transfer capacitance: $C_{rss} = C_{gd}$

The following figures show the parasitic capacitance.

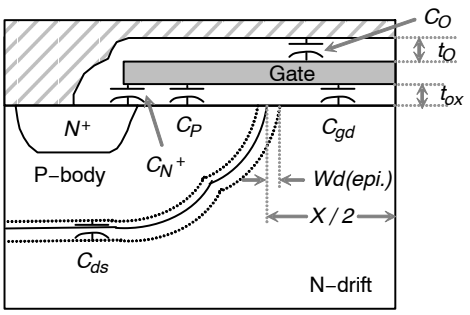


Figure 10. Vertical Structure, Parasitic Capacitance

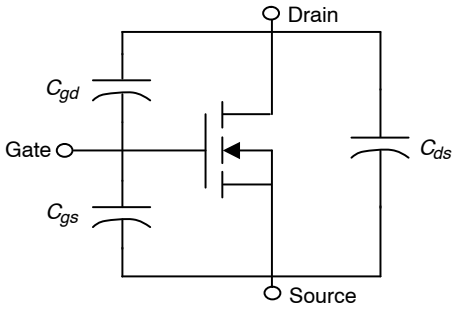


Figure 11. Equivalent Circuit, Parasitic Capacitance

C_{GS}: Capacitance between Gate and Source

$$C_{gs} = C_O + C_N + C_P$$

C_O is the capacitance between the gate and source metal:

$$C_O = \frac{\epsilon_I A_O}{t_O}$$

where

ε_I is the dielectric constant of the intervening insulator;

t_O is the thickness of the intervening insulator; and

A_O is the area of the overlap between the source and gate electrode.

C_{N^+} is the capacitance between the gate and the N^+ source diffusion region:

$$C_{N^+} = \frac{\epsilon_{ox} A_{N^+O}}{t_{ox}} = C_{OX} A_{N^+O}$$

where

ε_{ox} is the dielectric constant of the gate oxide;

t_{ox} is the gate oxide thickness;

C_{OX} is gate−oxide capacitance per unit area; and

A_{N^+O} is the area of overlap of the gate electrode over the N^+ emitter.

C_P is the capacitance between the gate and p−body. It is affected by the gate, the drain voltage, and the channel length. The C_P is the only component that is influenced by the change of the drain voltage (V_{DS}) among other Cgs components. When V_{DS} increases, the depletion region expands to the P−body and decreases the value of C_P. Even if the V_{DS} increases up to breakdown voltage, there is almost no change in the value of C_P, as the depletion region doesn't exceed 10% of the P−body. Hence, the change of C_{gs} due to V_{DS} is very small.

Cgd: Capacitance between Gate and Drain

This is influenced by the voltage of the gate and the drain. When there are variations in V_{DS}, the area under C_{gd} (n^-− drift region meeting with the gate oxide) is changed, and the value of the capacitance is affected. As shown in Equation 2, when $V_{DS} >> \phi_B$, the capacitance decreases as V_{DS} increases with the relation of $C_{gd} \propto \left(1 - k\sqrt{V_{DS}}\right)$.

$$C_{gd}\ (\text{per unit area}) = C_{OX}\left(1 - \frac{2W_{d(epi.)}}{X}\right) \quad \text{(eq. 2)}$$

where

X is the length between adjoining cells;

C_{OX} is gate−oxide capacitance per unit area;

$W_{d(epi.)}$ is the width of the depletion region in the epitaxial layer(= N− drift region); and

$$W_{d(epi.)} = \sqrt{\frac{2k_s \varepsilon_o (V_{DS} + \phi_B)}{q C_B}}$$

As C_{gd} increases ($1 + g_{fs}R_L$ (load resistance)) times due to the Miller effect, it prominently decreases the frequency characteristics.

Frequency Response of Power MOSFET

The frequency response of the power MOSFET is limited by the charging and discharging of the input capacitance. If the C_{gs} and C_{gd}, which determine the input capacitance, become smaller; it is possible to work in high frequency. As the input capacitance is unrelated to the temperature, the MOSFET's switching speed is unrelated to the temperature.

Cds: Capacitance between Drain and Source

The capacitance varies due to the variation of the C_{ds} thickness, which is the junction thickness of the P−body and the N^- drift region, with the change of V_{DS}:

$$C_{ds\ (per\ unit\ area)} = \sqrt{\frac{q\ k_s\ \varepsilon_o\ C_B}{2\left(V_{DS} + \phi_B\right)}}$$

where

- q is elementary electronic charge; (= 1.9×10^{-19} [C]) k_s = silicon dielectric constant;
- ε_o is the permeability of free space (8.86×10^{-14} [F/cm]);
- C_B is epitaxial layer background concentration [atoms / cm^3];
- V_{DS} is drain−to−source voltage; and
- ϕ_B is diode potencial.

As shown in the equation above, $V_{DS} >> \phi_B$ C_{ds} decreases as V_{DS} increases with the relationship of $C_{ds} \propto 1/\sqrt{V_{DS}}$.

Characteristics of the Gate Charge

It is the amount of charge required during MOSFET turn−on or turn−off transient.

The types of charges are:

- Total Gate Charge: Qg (The amount of charge during $t_0 \sim t_4$)
- Gate−Source Charge: Qgs (The amount of charge during $t_0 \sim t_2$)
- Gate−Drain (Miller) Charge: Qgd (The amount of charge during $t_2 \sim t_3$)

Figure 12 shows the gate−source voltage, gate−source current, drain−source voltage, and drain−source current during turn−on. They are divided into four sections to show the equivalent circuits at the diode−clamped inductive load circuit.

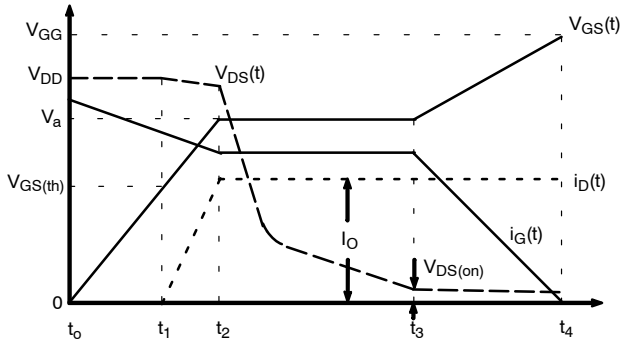
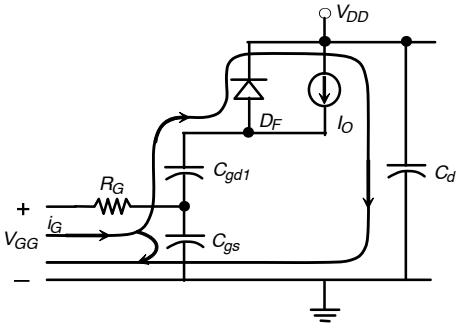
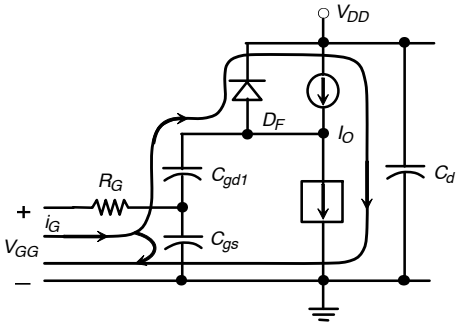


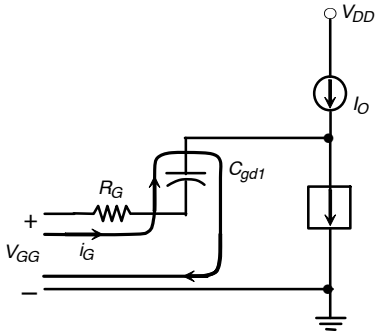
Figure 12. $V_{GS}(t)$, $I_G(t)$, $V_{DS}(t)$, $I_D(t)$ When Turned On



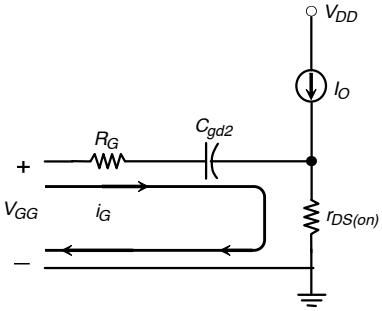
(a) $t_0 \sim t_1$ at the Diode−Clamped Inductive Load Circuit



(b) $t_1 \sim t_2$ at the Diode−Clamped Inductive Load Circuit



(c) $t_2 \sim t_3$ at the Diode−Clamped Inductive Load Circuit



(d) t_3 at the Diode−Clamped Inductive Load Circuit

Figure 13. Equivalent Circuits of the MOSFET with Turn−on Divided into 4 Periods at the Diode−clamped Inductive Load Circuit

$t_0 \sim t_1$

As I_G charges C_{gs} and C_{gd}, V_{GS} increases from 0 V up to $V_{GS}(th)$. The graph of increasing $V_{GS}(t)$ seems to be increasing linearly, but it is, in fact, an exponential curve having a time constant of $\tau_1 = R_G(C_{gs} + C_{gd1})$. As shown in Figure 13 (a), V_{DS} is still equal to V_{DD} and I_D is zero. The MOSFET is still in the turn−off state.

$t_1 \sim t_2$

V_{GS} increases exponentially, passing $V_{GS(th)}$, and, as V_{GS} continues to increase, I_D begins to increase and reaches full load current (I_O). So Va varies to I_O condition in t_2. When I_D is smaller than I_O and when it is in a state where the D_F is being conducted, V_{DS} maintains the V_{DD}. Figure 14 shows the voltage a little less than V_{DD}. This is caused by the voltage drop due to the existing inductance in the line.

Figure 14 shows the $V_{GS}(t)$ measuring the Va variation in accordance with i_D conditions in turn−on state.

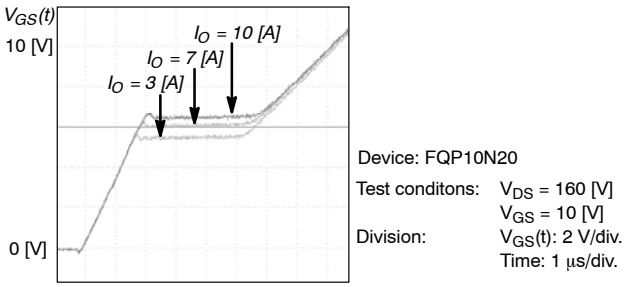


Figure 14. $V_{GS}(t)$ in Accordance with I_D Conditions

$t_2 \sim t_3$

V_{GS} is a constant value in accordance with the transfer characteristics as it is in an active region where I_D is the full load current (I_O). So, I_G can only flow through C_{gd} and is obtained by Equation 3.

$$i_G = \frac{V_{GG} - V_a}{R_G} \qquad \text{(eq. 3)}$$

V_{DS} can be configured as the following ratios:

$$\frac{dv_{DG}}{dt} = \frac{dv_{DS}}{dt} = \frac{i_G}{C_{gd}} = \frac{V_{GG} - V_a}{R_G C_{gd}} \qquad \text{(eq. 4)}$$

This is the region where the MOSFET is still operating in the active region and, as the V_{DS} decreases, it gets closer to the ohmic region. When V_{DD} increases, $t_2 \sim t_3$ (flat region of V_{GS}) also increase.

Figure 15 graphs $V_{GS}(t)$ and shows the variation of $t_2 \sim t_3$ (flat region of V_{GS}) in accordance with the V_{DD} condition.

At t_3, V_{DS} becomes $V_{DS(on)}$=IO · $R_{DS(on)}$ and the transient is completed. The MOSFET is placed at the boundary of entering the ohmic region from the active region.

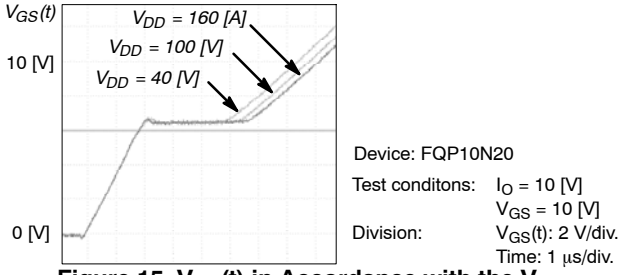


Figure 15. $V_{GS}(t)$ in Accordance with the V_{DD} Condition

$t_3 \sim t_4$

$t_3 \sim t_4$ is the period where it operates in an ohmic region. The V_{GS} increases up to V_{GG} with a time constant of $\tau_2 = R_G (C_{gs} + C_{gd2})$.

Drain−Source On Resistance ($R_{DS(on)}$)

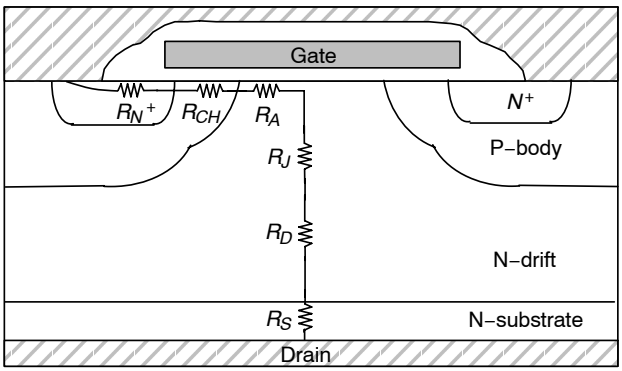


Figure 16. The Vertical Structure of a MOSFET Showing Internal Resistance

In a MOSFET, $R_{DS(on)}$ is the total resistance between the source and the drain during the on state. It is an important parameter, determining maximum current rating and loss. To reduce $R_{DS(on)}$, the integrity of the chip and trench technique are used. This can be stated as in Equation 5:

$$R_N{}^+ + R_{CH} + R_A + R_j + R_D + R_S \qquad \text{(eq. 5)}$$

where

$R_N{}^+$ The resistance of the source region with N^+ diffusion. It only uses a small portion of resistance compared to other components that form $R_{DS(on)}$. It can be ignored in high−voltage power MOSFETs.

R_{CH} The resistance of the channel region, which is the dominant $R_{DS(on)}$ factor in low−voltage MOSFETs. This resistance can be varied by the ratio of the channel's width to the length, the

thickness of the gate oxide, and the gate drive voltage.

R_A As the gate drive voltage is supplied, charges start to accumulate in N^- epi surface (the plate under C_{gd}) and forms a current path between the channel and the JFET region. The resistance of this accumulation region is R_A. The resistance varies by the charge in the accumulation layer and the mobility of the free carriers at the surface. If the gate electrode is reduced, its effect is the same as reducing the length of the accumulation layer, so the value of RA is reduced while R_J increases.

R_J The N^- epi region between the P−bodies is called the JFET region because the P−body region acts like the gate region of a JFET. The resistance of this region is R_J.

R_D The resistance occurring from right below the P−body to the top of the substrate is R_D and is the most important factor in high−voltage MOSFETs.

R_S The resistance of the substrate region. It can be ignored in high−voltage MOSFETs. In low−voltage MOSFETs, where the breakdown voltage is below 50 V, it can have a large effect on $R_{DS(on)}$.

Additional resistances can arise from non−ideal contact between the source/drain metal and the N^+ semiconductor regions, as well as from the leads used to connect the device to the package.

$R_{DS(on)}$ increases with the temperature (positive temperature coefficient) because the mobility of the hole and electron decreases as the temperature rises. The $R_{DS(on)}$, at a given temperature of a P/N−channel power MOSFET can be estimated with the following equation.

$$R_{DS(on)}(T) = R_{DS(on)}(25°C)\left(\frac{T}{300}\right)^{2.3} \quad \text{(eq. 6)}$$

where

T is absolute temperature.

This is an important characteristic of device stability and paralleling. It doesn't need any external circuit assistance to have good current sharing when $R_{DS(on)}$ increases with the temperature and is connected in parallel.

Threshold Voltage ($V_{GS(th)}$)

This is the minimum gate bias that enables the formation of the channel between the source and the drain. The drain current increases in proportion to $(V_{GS} - V_{GS(th)})^2$ in the saturation region.

High $V_{GS(th)}$

It is difficult to design gate drive circuitry for the power MOSFET because a high gate bias voltage is needed to turn it on.

Low $V_{GS(th)}$

When the $V_{GS(th)}$ of the N−channel power MOSFET becomes negative due to the existence of charges in the gate oxide, it shows the characteristics of a normally on state, where the conductive channel exists even in a zero− gate bias voltage. Even if $V_{GS(th)}$ is positive and the value is very small, there could be a turn−on either by the noise signal of the gate terminal or by the increasing gate voltage during high−speed switching.

$V_{GS(th)}$ can be controlled by the gate oxide thickness. Normally, gate oxide is kept thick in a high−voltage device so the $V_{GS(th)}$ is set at 2 V ~ 4 V. Gate oxide is kept thin in a low−voltage device (logic level) so $V_{GS(th)}$ is 1 V ~ 2 V. Additionally, $V_{GS(th)}$ can be controlled by background doping (the density of P−body for the N−channel power MOSFET). It increases in proportion to the square root of the background doping.

Temperature Characteristic

$V_{GS(th)}$ decreases as the temperature increases. The rate of decrease can be varied by the gate oxide thickness and background doping level. In other words, the decrease rate increases when the gate oxide becomes thicker and the background doping level increases.

Transconductance (g_{fs})

Transconductance is the gain in the MOSFET, expressed in Equation 7. It represents the change in drain current by the change in the gate−source bias voltage:

$$g_{fs} = \left[\frac{\Delta I_{DS}}{\Delta V_{GS}}\right]_{V_{DS}} \quad \text{(eq. 7)}$$

V_{DS} should be set so that the device can be activated in the saturation region. V_{GS} should be supplied so that the I_{DS} becomes half of the maximum current rating. gfs varies depending on the channel width/length and the gate oxide thickness. As shown in Figure 17, after $V_{GS(th)}$ is applied, g_{fs} increases dramatically with the increase in the drain current and becomes a constant after drain current reaches a certain point (at higher values of drain current). If g_{fs} is high enough, high current handling capability can be gained from the low gate drive voltage. High−frequency response is also possible.

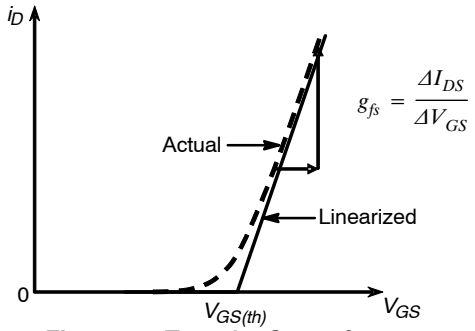


Figure 17. Transfer Curve & g_{fs}

Temperature Characteristic

g_{fs} decreases as the temperature increases due to the reduction of mobility. Equation 8 is similar to the $R_{DS(on)}$ and temperature relationship; it is possible to know the gfs changes by the changes in temperature:

$$g_{fs}(T) = g_{fs}(25°C)\left(\frac{T}{300}\right)^{-2.3} \quad \text{(eq. 8)}$$

where

T is absolute temperature.

Drain−Source Breakdown Voltage (BV_{DS} Breakdown Voltage Temperature Coefficient ($\Delta BV/\Delta TJ$)

BV_{DSS} is the maximum drain−to−source voltage where the MOSFET can endure without the avalanche breakdown of the body−drain pn junction in off state (where the gate and source are shorted). The measurement conditions are V_{GS} = 0 V, I_D = 250 μA, and the length of the drift region (N^- epitaxy) is determined by the BVDSS. Avalanche, reach− through, punch−through, Zener, and dielectric breakdowns are the factors that drive breakdown.

Temperature Characteristic

As junction temperature increases, it does so linearly. Whenever it goes up 100°C, 10% of BV_{DSS} at 25°C increases *(refer to the breakdown voltage temperature coefficient (ΔBV/ΔTJ) and Figure 18 breakdown voltage vs. temperature)*.

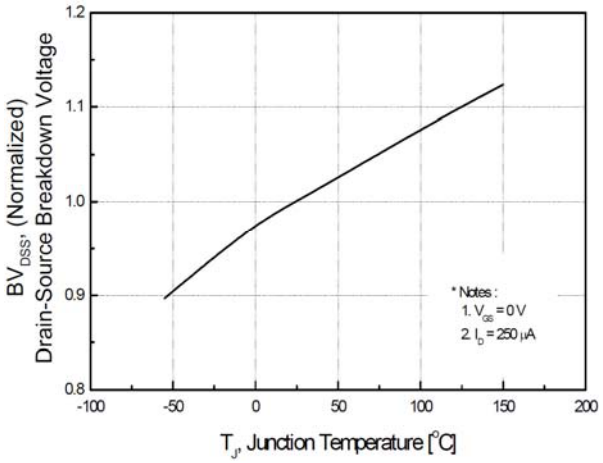


Figure 18. Breakdown Voltage vs. Temperature

Drain−to−Source Leakage Current (I_{DSS})

I_{DSS} can be measured by providing the maximum drain−to− source voltage and 80% of the voltage (T_C = 125°C) in the off state, where the gate is shorted to the source. I_{DSS} is more sensitive to the temperature than BV_{DSS} and it has a positive temperature coefficient.

Gate−to−Source Voltage (V_{GS})

V_{GS} represents the maximum operating gate−to−source voltage. The negative voltage handling capability enables the enhancement of the turn−off speed by providing reverse bias to the gate and the source.

Gate−Source Leakage, Forward / Reverse (I_{GSS})

I_{GSS} is measured by providing the maximum operating gate− to−source voltage (V_{GS}) between the gate and the source. Forward or reverse direction is determined by the polarity of the V_{GS}. I_{GSS} is dependent on the quality of the gate oxide and device size.

Switching Characteristics ($t_{d(on)}$, t_r, $t_{d(off)}$, t_f)

Power MOSFETs have good switching characteristics as there is no storage delay caused by the minority carrier and no variation caused by the temperature. Figure 19 shows the switching sequence divided into sections.

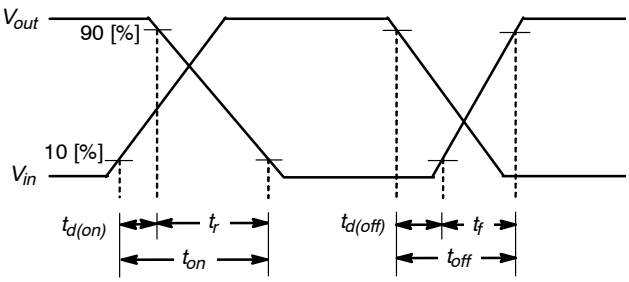


Figure 19. Resistive Switching Waveforms

Table 2. SWITCHING CHARACTERISTICS

Turn−On Delay ($t_{d(on)}$):	This is the time for the gate voltage, V_{GS}, to reach the threshold voltage $V_{GS(th)}$. The input capacitance during this period is Cgs+Cgd. This means that this period is the charging period to bring up the capacitance to the threshold voltage.
Rise Time (t_r):	It is the period after the V_{GS} reaches $V_{GS(th)}$ to complete the transient. It can be divided into two regions. One is the period where the drain current starts from zero (increasing with the gate voltage in accordance with the transfer characteristics) and reaching the load current. The other region is when the drain voltage starts to drop and reaches the on−state voltage drop. As shown in the gate charge characteristics graph, the V_{GS} maintains a constant value as the drain current is constant in this region where the voltage decreases. During the rise time, as both the high voltage and the high current exist in the device, high power dissipation occurs. The rise time should be reduced by reducing the gate series resistance and the drain−gate capacitance (C_{gd}). After this, the gate voltage continues to increase up to the supplied voltage level; but, as the drain voltage and the current are already in steady state, they are not affected during this region.
Turn−Off Delay ($t_{d(off)}$):	The gate voltage operates in the supplied voltage level during On state and, when the turn− off transient starts, it starts to decrease. The $t_{d(off)}$ is the time for the gate voltage to reach the point where it is required to make the drain current become saturated at the value of load current. During this time, there are no changes to the drain voltage and the current.
Fall Time (t_f):	Fall time is the time where the gate voltage reaches the threshold voltage after $t_{d(off)}$. It is divided into the region where the drain voltage reaches the supply voltage from On−state voltage and the region where the drain current reaches zero from the load current. As there is a lot of power dissipation in the tr region during turn−on state, the power dissipation occurs in the tf region during turn−off state. Hence, t_f must be reduced as much as possible. After this, the gate voltage continues to decrease until it reaches zero. As the drain voltage and the current are already in steady state, they are not affected during this region.

Single−Pulsed Avalanche Energy Unclamped Inductive Switching (E_{AS})

MOSFET Turn−Off (Inductive Load Circuit)

While in on state (supplying positive voltage exceeding the threshold voltage in N−channel device), the electrons flow into the drain from the source through the inversion layer (= channel) of the body surface and form a current flow from the drain to the source. If it is an inductive load, this current increases linearly. To turn off the MOSFET, the gate voltage must be removed or a reverse voltage applied so that it eliminates the inversion layer of the body surface. Once the charge at the inversion layer begins to dissipate and the channel current (drain current) begins to reduce, the inductive load increases the drain voltage so that it maintains the drain current. When the drain voltage increases, the drain current is divided into the channel current and the displacement current. Displacement current is the current generated as the depletion region is developed at the drain−body diode and it is proportional to dv_{DS}/dt (the ratio of drain voltage rise by the time). The dv_{DS}/dt is limited by how fast the gate is discharged and by how fast the drain−body depletion region is charged. The charge of the drain−body depletion region is determined by C_{ds} and the magnitude of the drain current. When the drain voltage increases and cannot be clamped by an external circuit UIS (Unclampled Inductive Switching), the drain−body diode starts to build the current carriers through avalanche multiplication and the device falls into a Sustaining Mode. While in Sustaining Mode, all the drain current (avalanche current) goes through the drain−body diode and is controlled by the (channel current equals to zero) inductor load. If the current (leakage current, displacement current (dv_{DS}/dt current), and avalanche current) flowing at the body region underneath the source is large enough; the parasitic bipolar transistor becomes active and can result in device failure.

Figure 20 shows the drain voltage and the current when a single pulse (width: t_P) is supplied at the unclamped inductive load circuit.

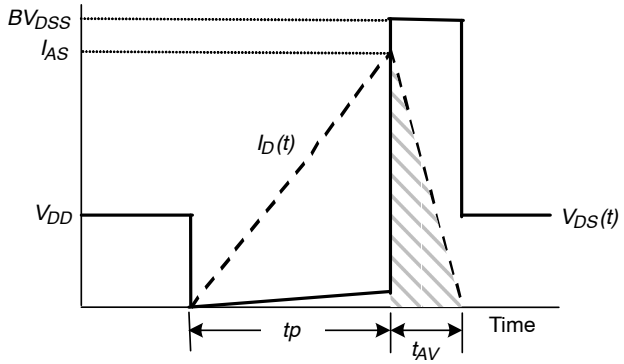


Figure 20. Unclamped Inductive Switching Waveforms

$I_D(t)$ can be changed by the inductor load size, supply voltage (V_{DD}), and the gate pulse width (t_P). The shaded area of the avalanche region (t_{AV}) shows the dissipation energy (E_{AS}). Calculate E_{AS} and t_{AV} with Equation 9:

$$E_{AS} = \frac{1}{2} L_L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

$$t_{AV} = \frac{L_L I_{AS}}{BV_{DSS}} \quad \text{(eq. 9)}$$

Power MOSFET Failure Characteristics during Inductive Turn−Off

It has the same electrical characteristics as the second breakdown of the bipolar transistor. It is independent from dv_{DS}/dt. By maintaining the gate turn−off voltage constantly and changing the magnitude of the external gate resistance, the magnitude of the gate turn−off current changes. This changes the dV_{DS}/dt. If dV_{DS}/dt current causes a device failure, the voltage that can lead to a second breakdown should be decreased with an increase in dV_{DS}/dt. When measuring the second breakdown voltage while changing the external gate resistance (changing dV_{DS}/dt), the highest voltage should be measured at the highest dV_{DS}/dt *(according to "Turn−Off Failure of Power MOSFETs," by David L. Blackburn)*. The voltage at which failure occurs increases with temperature. Critical current reduces as temperature increases. Critical current represents the maximum value of the drain current that can safely turn off the device in an unclamped mode. At currents exceeding this, a second breakdown occurs. It is not related to the magnitude of the load inductance. The avalanche current from the drain−body diode activates the parasitic bipolar transistor. This causes the MOSFET to fail.

Repetitive Avalanche Rating (E_{AR}, I_{AR})

E_{AR}

It represents avalanche energy for each pulse under repetitive conditions.

I_{AR}

It represents the maximum avalanche current and is the same as the I_D rating of the device.

Drain−to−Source dv/dt Ratings

When high dv/dt is supplied at the drain, there is a possibility of current conduction in the power MOSFET. In some cases, this can destroy the device. Below are some instances of device turn−on due to dv/dt.

Static dv/dt

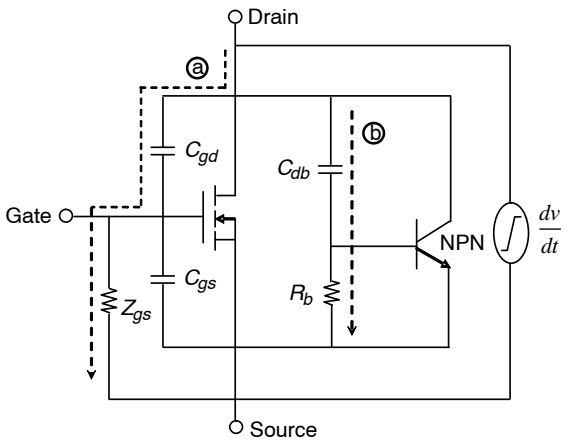


Figure 21. Equivalent Circuit of a N−Channel MOSFET

False Turn−on

In off state, a sudden increase in drain voltage changes the voltage across the parasitic capacitance between the drain and the gate and develops displacement current (a) of Cdv/ dt. If voltage exceeding $V_{GS(th)}$ develops between the gate and source due to the displacement current and the gate−to− source impedance (Z_{gs}), it triggers a false turn−on of the MOSFET. The parasitic capacitance between the drain and gate can be C_{gd} or larger than C_{gd}, depending on the circuit layout. Z_{gs} is the impedance of the drive circuit and can be presented as a series of R, L battery components. Due to the false turn−on, the device falls into a current−conduction state and, in severe cases, high power dissipation develops in the device and results in destructive failure. Equation 10 shows the voltage drop V_{GS} across Z_{gs}, and dv/dt capability in this mode:

$$V_{GS} = Z_{gs}\, C_{gd} \left[\frac{dv}{dt}\right]$$

$$\left[\frac{dv}{dt}\right] = \frac{V_{GS(th)}}{Z_{gs}\, C_{gd}} \qquad \text{(eq. 10)}$$

To increase dv/dt capability, a gate drive circuit with very low impedance should be used and $V_{GS(th)}$ must be increased. In a drive circuit with low impedance, the cost is high and increasing the $V_{GS(th)}$ is associated with rise in $R_{DS(on)}$. As $V_{GS(th)}$ has a negative temperature coefficient, the possibility of a false turn−on increases as the temperature rises. Typically, gate voltage doesn't go over the threshold voltage and the high device resistance limits the device current. Device destruction due to false turn−on is rare.

Parasitic Transistor Turn−on

In off state, a sudden increase in drain voltage changes the voltage across C_{db}, and it develops current (b) flowing through R_b. When the voltage across the R_b goes over V_{be} (emitter−base forward bias voltage where the parasitic bipolar transistor is turned on, approximately 0.7 V), the parasitic bipolar transistor is turned on. When the parasitic bipolar transistor is turned on, the breakdown voltage of the device is reduced from BV_{CBO} to BV_{CEO}, which is 50 ~ 60% of BV_{CBO}. If a drain voltage larger than BV_{CEO} is supplied, the device falls into an avalanche breakdown. If this drain current is not limited externally, the device can be destroyed by the second breakdown. The following equation shows the dv/dt capability in this mode:

$$\left[\frac{dv}{dt}\right] = \frac{V_{be}}{R_b\, C_{db}} \qquad \text{(eq. 11)}$$

Equation 11 reveals that the dv/dt capability is determined by the internal device structure. For high−dv/dt capability, the R_b value must be small. This is achieved by increasing the doping level of the P−body region and reducing the length of the N^+ emitter as much as possible. R_b is also affected by the drain voltage. As the drain voltage increases, the depletion layer expands and enlarges the R_b value. When

the temperature rises, R_b is increased by the reduction of mobility. As the V_{be} decreases, the possibility of turn−on of the parasitic transistor increases. As the base and the emitter are shorted by the source contact, the R_b value is very small. This occurs only if the dv/dt is enormously large.

In a false turn−on, the dv/dt can be controlled externally. In a parasitic transistor's turn−on, the dv/dt is determined by device design. This is the difference between these modes.

Dynamic dv/dt

If there is a sudden current interruption, such as a clamped inductive turn−off in high−speed switching, the device is destroyed by concurrent stresses caused by high drain current, high drain−source voltage, and displacement current at the parasitic capacitance.

Diode Recovery dv/dt

This is the main cause of dv/dt failure in specific applications, such as circuits using a body drain diode. The datasheet gives the maximum value for dv/dt. Exceeding this value causes device failure due to excessive diode recovery dv/dt. Figure 22 shows a motor control circuit application with a diode recovery dv/dt problem.

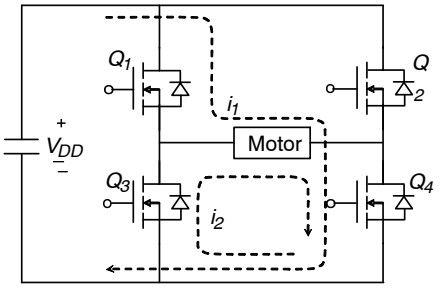


Figure 22. Motor Control Circuit

First Q_1 and Q_4 are conducted and put in a state where current I_1 passes. If Q_1 is turned off to control the speed of the motor, the current flows through the parasitic diode (freewheeling diode) of Q_3 as I_2. The parasitic diode of Q_3 falls into a forward bias state and, due to the characteristic of the diode, the minority charge begins to accumulate. When Q_1 is turned on, the current again becomes I_1 and the minority charge accumulated in the parasitic diode, Q_3, is removed by the diode reverse−recovery current (Figure 23 section a of I_S). Once the minority charge is removed to a certain level, the depletion region of the body drain diode expands and makes more reverse−recovery current (Figure 23 section b of I_S). If this turns on the parasitic bipolar transistor, Q3 is destroyed. Figure 23 and Figure 24 show the diode recovery dv/dt test circuit and waveforms. From this test; dv/dt, V_{SD} (diode forward voltage), t_{rr} (reverse− recovery time), and Q_{rr} (reverse−recovery charge) data can be obtained. In the test, the V_{DD} value must be less or equal to the BV_{DSS}. Typically, the V_{DD} is set at 80% of BV_{DSS} and the pulse period of the driver V_{GS} must be controlled so that the I_S can become the continuous drain current I_D.

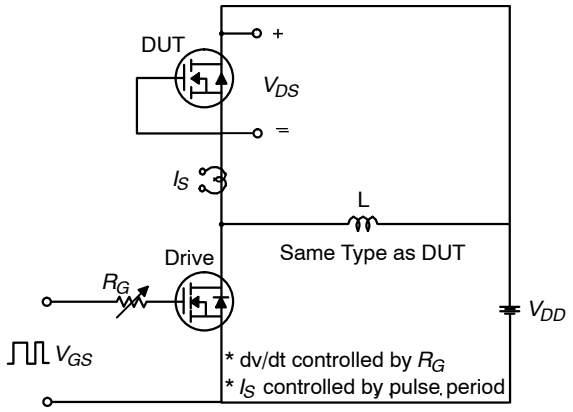


Figure 23. Diode Recovery dv/dt Test Circuit

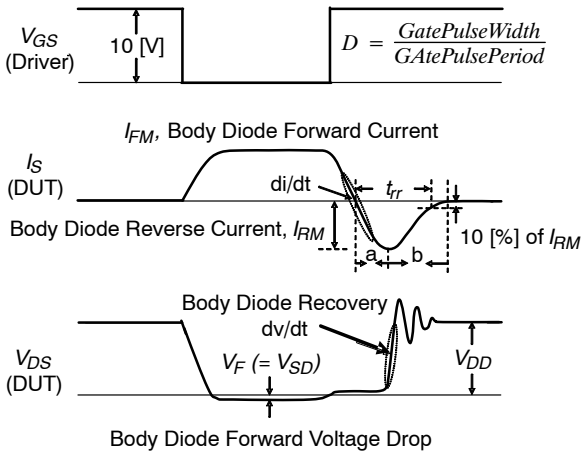


Figure 24. Diode Reverse Recovery Waveforms

The value of di/dt and dv/dt becomes larger as R_G is reduced. t_{rr} can be obtained by measuring the part shown in the wave of I_S where the di/dt (measured from the point where it is 50% of I_{FM} above the ground to the point where it is 75% of I_{RM} below the ground) is 100 A/μs. Q_{rr} can be calculated as $(I_{RM} \times t_{rr})/2$. dv/dt can be measured from the point where it is between 10~90% of V_{DD} with the di/dt condition (measured from the point where it is 50% of I_{FM} above the ground to the point where it is 75% of I_{FM} below the ground). I_S (continuous source current) and I_{SM} (pulsed – source current) represent the current rating of the source−drain diode, $I_S = I_D$ (continuous drain current), and $I_{SM} = I_{DM}$ (drain current – pulsed).

Thermal Characteristics (T_J, $R_{\theta JC}$, $R_{\theta SA}$, $Z_{\theta JC}(t)$)

The power loss of the device turns into heat and increases the junction temperature. This degrades device characteristics and reduces its life span. It is very important to lower the junction temperature by discharging heat from the chip junction. The thermal impedance ($Z_{\theta JC}(t)$) is used to monitor the above.

Thermal characteristics terminology:

- Junction Temperature (T_J)

- Case Temperature (T_C): Temperature at a point of the package that has the semiconductor chip inside.
- Heat Sink Temperature (T_S)
- Ambient Temperature (T_A): Temperature of the surrounding environment of the operating device.
- Junction−to−Case Thermal Resistance ($R_{\theta JC}$)
- Case−to−Sink Thermal Resistance ($R_{\theta CS}$)
- Sink−to−Ambient Thermal Resistance ($R_{\theta SA}$)

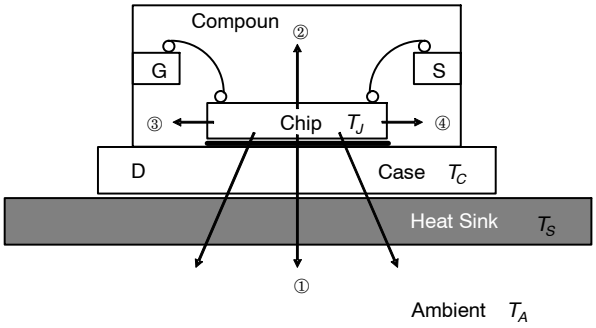


Figure 25. Thermal Discharge Path at Chip Junction

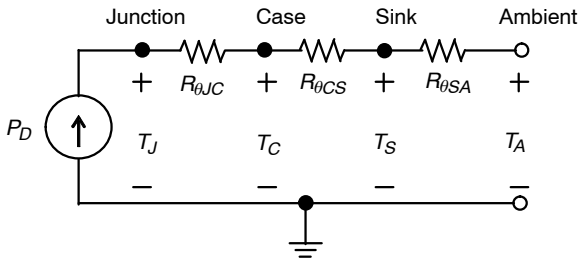


Figure 26. Circuit Based on Thermal Resistance

As shown in Figure 25, the heat produced at the chip junction normally discharges over 80% in the direction of ① and about 20% in the direction of ②③④. The path of the thermal discharge is the same as the movement of the current and is represented in Figure 26 after considering thermal resistance. This is true only for DC operation. Most MOSFETs are used in switching operations with a fixed duty factor. Thermal capacitance should be taken into consideration, along with thermal resistance. The thermal resistance from the chip junction to the ambient is $R_{\theta JA}$ (junction−to−ambient thermal resistance) and the equivalent circuit can be expressed as Equation 12.

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad \text{(eq. 12)}$$

Junction−to−Case Thermal Resistance ($R_{\theta JC}$)

$R_{\theta JC}$ is the internal thermal resistance from the chip junction to the package case. Once the size of the die is decided, this thermal resistance of pure package is only determined by the package design and lead frame material. $R_{\theta JC}$ can be measured under the condition of T_C = 25°C and can be written as Equation 13:

$$R_{\theta JC} = \frac{T_J - T_C}{P_D} \ [°C/W] \quad \text{(eq. 13)}$$

Condition T_C = 25°C means the infinite heat sink is mounted.

Infinite heat sink means the case temperature of the package is equal to the environment temperature. It is the heat sink, which can realize $T_C = T_A$.

Case−to−Sink Thermal Resistance ($R_{\theta CS}$)

This is the thermal resistance from the package case to the heat sink. It can vary due to the package and the mounting method to the heat sink.

Case−to−Ambient Thermal Resistance ($R_{\theta CA}$)

This is the thermal resistance from the heat sink to the ambient and it is determined by heatsink design.

Thermal Response Characteristics

Figure 27 shows the thermal response curve. As show in Figure 27, the graph of the thermal response, shows the change of junction−to−case thermal impedance ($Z_{\theta JC}(t)$) due to the change of the square−wave pulse duration with a few duty factor conditions. $Z_{\theta JC}(t)$ determines the junction temperature rise with the Equation 14. (considering power dissipation to be a constant value (P_{DM}) during the conduction period, it becomes saturated to the maximum value of ($R_{\theta JC}$) as it reaches low frequency or DC operation where the duty factor D = 1. Figure 28 shows the junction temperature rise with the increasing duty factor.

$$T_{Jmax} - T_C = R_{\theta JC} \cdot P_{DM} \quad \text{(eq. 14)}$$

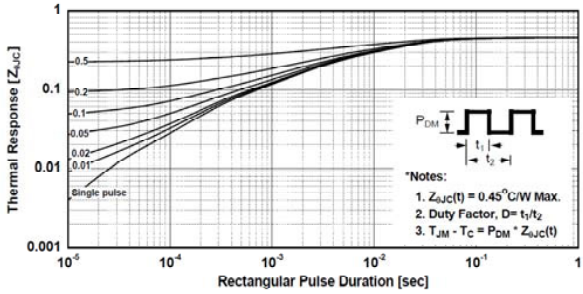


Figure 27. Transient Thermal Response Curve

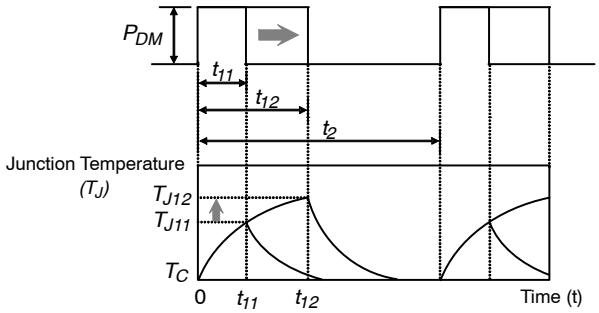


Figure 28. Resistance; Charge in Junction Temperature due to Conduction Time

A single−pulse curve determines the thermal resistance for repetitive power pulses having a constant duty factor (D), as shown in Equation 15.

$$R_{\theta JC}(t) = R_{\theta JC} \cdot D + (1 - D) \cdot S_{\theta JC}(t) \quad \text{(eq. 15)}$$

where

$Z_{\theta JC}(t)$ is the thermal impedance for repetitive power pulses with a duty factor of D;

$S_{\theta JC}(t)$ is the thermal impedance for a single pulse;

I_D is continuous drain current; and

I_{DM} is drain current, pulsed.

As shown in Equation 16, the I_D rating is determined by the heat removal ability of the device. Figure 10 in the datasheet, maximum drain current vs. case temperature, shows increasing permissible I_D as T_C decreases.

$$I_D(T_C) = \sqrt{\frac{T_{Jmax} - T_C}{R_{DS(on)}(T_{Jmax}) \cdot R_{\theta JC}}} \quad \text{(eq. 16)}$$

where

$R_{DS(on)}(T_J max)$ is the maximum value of on−resistance in an appropriate drain current condition ($\frac{1}{2} \cdot I_D$ in datasheet) at $T_{Jmax.}$ as maximum $R_{DS(on)}$ specified is at T_C = 25°C.

$R_{DS(on)}$ (T_{Jmax}) could be analogized by the graph of on−resistance vs. temperature;

$R_{\theta JC}$ is maximum junction−to−case thermal resistance; and

T_C is case temperature.

In real device applications where it is not feasible to maintain the temperature at T_C = 25°C, the I_D (60 ~ 70% of I_D at T_C = 25°C) at T_C = 100°C is a more usable specification.

Drain Current − Pulsed (I_{DM})

The drain current over continuous drain current rating should not go over the maximum junction temperature. The maximum upper limit is I_{DM}. I_{DM} is about four times the value of I_D, as shown in Equation 17.

$$I_{DM} = I_D\,(T_C = 25[°C]) \times 4 \quad \text{(eq. 17)}$$

Repetitive rating: Pulse width limited by maximum junction temperature.

Total Power Dissipation (P_D), Linear Derating Factor

$$P_D(T_C) = I_D^2(T_C) \cdot R_{DS(on)}(T_{Jmax}) = \frac{T_{Jmax} - T_C}{R_{\theta JC}} \quad \text{(eq. 18)}$$

Linear derating factor is calculated by:

$$\frac{1}{R_{\theta JC}} \quad \text{(eq. 19)}$$

Safe Operating Areas (SOA)

SOA (FBSOA)

It defines the maximum value of the drain−source voltage and drain current that guarantees safe operation when the device is at the forward bias.

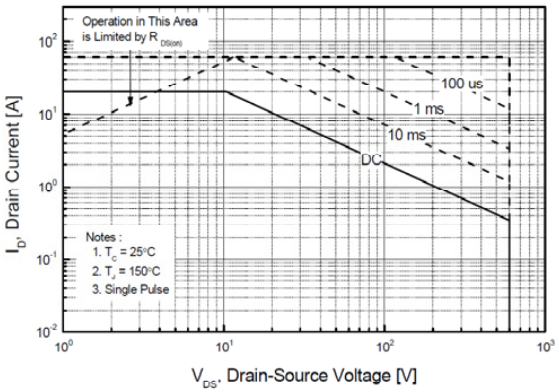


Figure 29. Maximum Safe Operating Area

Boundaries

Figure 29 shows the maximum safe operation area.

In Figure 29, the right line: maximum drain−source voltage rating.

The horizontal line: DC is the maximum rated continuous drain current at T_C = 25°C. For MOSFETs, excluding package limitations, maximum rated continuous drain current can be determined by the $R_{DS(on)}(T_{Jmax})$, as in Equation 20.

$$I_D(T_C) = \sqrt{\frac{T_{Jmax} - T_C}{R_{DS(on)}(T_{Jmax}) \cdot R_{\theta JC}}} \quad \text{(eq. 20)}$$

Single pulse is the maximum rated drain current, pulsed:

$$I_{DM} = I_D(T_C) \times 4 \quad \text{(eq. 21)}$$

The Upper Limit with Positive (+) Slope

The boundary where the power can be limited by the drain− to−source on resistance.

The Upper Limit with Negative (−) Slope

It is determined by the transient thermal impedance and the maximum junction temperature.

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